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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,401	01/11/2002	Eric R. DeLano	10016664-1	8893
22879	7590	01/05/2006	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			LEE, CHRISTOPHER E	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 01/05/2006

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/044,401

Filing Date: January 11, 2002

Appellant(s): DELANO, ERIC R.

Roger D. Greer (Reg. No. 26,174)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 30th of September 2005 appealing from the Office action mailed on 18th of January 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying no related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following ground of rejection is not presented for review on appeal because it has been withdrawn by the Examiner. The Appellant's arguments with respect to claims 12, 16, and 17 rejection under 35 U.S.C. §112, second paragraph have been fully considered and are persuasive, and thus the rejection of claims 12, 16, and 17 under 35 U.S.C. §112, second paragraph has been withdrawn.

Therefore, the grounds of rejection to be reviewed on appeal are as follows:

- Whether the §102(b) rejection of claims 1, 3, 6-8 and 11-13 based on Yokoyama (JP 411296473) should be reversed because of the Examiner's misinterpretation of Yokoyama?
- Whether the §103 rejection of claims 16 and 17 should be reversed as being based upon the misinterpretation of Yokoyama in combination with Lach?

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon**Applicant's Admitted Prior Art**

JP 411296473 A	Yokoyama	10-1999
US 6,411,230 B1	Tauchen et al.	6-2002
US 6,570,876 B1	Aimoto	5-2003
US 5,717,871 A	Hsieh et al.	2-1998
US 6,363,452 B1	Lach	3-2002

Examiner's Note :

- The Examiner referred to Yokoyama [JP 411296473 A] reference, which had been filed via IDS by the Appellant on 11th of July 2003, as a prior art for the claim rejections in the Office Action, and it was referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner provided a machine translated copy of the reference for the convenience of the Appellant. However, the Examiner cautioned the Appellant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.
- The Examiner officially acquired a human translation of the full-version Yokoyama in English by request to the Office for the purpose of submitting to the Board of Patent Appeals and Interferences, and the full-version Yokoyama in English is attached.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, 6-8 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yokoyama [JP 411296473 A; cited by the Applicant].

Referring to claim 1. Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) for providing connections between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising:

- a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being
 - an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and
 - an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and,
- crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example),
 - said crossbar control data (i.e., discernment bits Sa and Sb, and Address) containing control information for formatting bit length of data (i.e., control information for

configuring 128 bit or 256 bit port; See Fig. 24) from an input port (e.g., port for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as an input port, such that SW#2 being set ‘1’ and SW#3 being set ‘1’ make the port configure as an input port according to Figs. 3 and 11) to be transmitted to an output port (e.g., port for DA I/O Board #1-#4 in Fig. 1 configured as an output port, such that SW#2 being set ‘0’ and SW#3 being set ‘0’ make the port configure as an output port according to Figs. 3 and 11) having less width than said input port (e.g., 256 bit board → 128 bit board in Fig. 24; See Paragraph [0149]).

Referring to claim 3, Yokoyama teaches

- at least one register (i.e., memory A 61-b1 and memory B 61c-1 in Fig. 9) on each input port and each said output port for storing data in memory (i.e., storing configuration environment of the crossbar switch in the memory A, and partner’s board name and port number in the memory B; See paragraphs [0076]-[0077]).

Referring to claim 6, Yokoyama teaches

- an input port and an output port (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set ‘1’ and SW#3 being set ‘1’ making the port configure as an input port, and ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set ‘0’ and SW#3 being set ‘0’ making the port configure as an output port according to Figs. 3 and 11) of at least one of said plurality of ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1) are customized to have different widths (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 7, Yokoyama teaches

- a plurality of said input ports (e.g., ports for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as input ports, such that SW#2 being set ‘1’ and SW#3 being set ‘1’ make the port configure as an input port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 8, Yokoyama teaches

- a plurality of said output ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set ‘0’ and SW#3 being set ‘0’ make the port configure as an output port according to Figs. 3 and 11) are customized to have different width (i.e., 128 bit and 256 bit port configurations; See Fig. 24).

Referring to claim 11, Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1) having a plurality of paths for providing connections (i.e., a plurality of communication paths among Processor Boards #1-#2, Memory Boards #1-#2 and DA I/O Board #1-#4 in Fig. 1) between a plurality of ports (e.g., DA I/O Board #1-#4 in Fig. 1) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) via a processing system (i.e., Crossbar Switch 5, Crossbar Switch I/O ports 6, Address Controller 8 and Data division 7 in Fig. 1) comprising:

- a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being
 - an input port customized (See Figs. 3 and 11; i.e., SW#2 being set ‘1’ and SW#3 being set ‘1’ make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and

- an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1);
- a plurality of virtual communication channels (i.e., data paths by the interconnection of switches in Fig. 5) on each input port (i.e., on each data division 7-1 of Fig. 3); and,
- crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from a virtual communication channel to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example).

Referring to claim 12, Yokoyama discloses a method for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2, Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1); and, crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port

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to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), said method comprising the steps of:

- receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3);
- obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively);
- determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration);
- obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13);
- processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]);
- determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board);

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- submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data);
- obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example);
- formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]);
- submitting said formatted data as said processed data; and,
- transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Referring to claim 13, Yokoyama teaches

- reading control data received with said data on said input port (See Box S1 in Fig. 12 and col. 15, lines 41-45);
- determining whether said control data have valid port information (See Decision Box S2 in Fig. 12 and Decision Box S14 in Fig. 13 and paragraph [0098]; i.e., if a bit configuration information in said control data is not confirmed by OK from address line, then said control data has an invalid port information) and,

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- aborting when said control data does not have valid port information (See Decision Box S16 and Box S17 in Fig. 13 and paragraph [0099]).

Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Applicant's Admitted Prior Art [hereinafter AAPA].

Referring to claim 2. Yokoyama discloses all the limitations of the claim 2, including said data received on said input port including control data for indicating destination information relating to data received on said input port (See paragraph [0080]), except that does not teach said data further comprising control data for indicating validity information relating to said data.

AAPA discloses a crossbar (Fig. 1), wherein

- said crossbar using control information from control data, which indicates validity information relating to data received on an input port (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

Referring to claim 14. Yokoyama discloses all the limitations of the claim 14, including obtaining said destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) from said control data (See paragraph [0080]), except that does not expressly teach said obtaining is performed when said control data has valid port information.

AAPA discloses a crossbar (Fig. 1), wherein

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- obtaining a destination output port from said control data when said control data has valid port information (See page 5, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said validity information, as disclosed by AAPA, in said data received on said input port, as disclosed by Yokoyama, so as to verify the validity of port information relating to said data received on said input port, which is admitted by the applicant as well-known in the art (See AAPA, page 5, lines 13-19).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Tauchen et al. [US 6,411,230 B1; hereinafter Tauchen].

Referring to claim 4, Yokoyama discloses all the limitations of the claim 4, except that does not expressly teach at least one shift register on each input port for storing data in memory and shifting data with larger bit length to a smaller bit length data for transmission from an input port with more width to an output port with less width.

Tauchen discloses a circuit arrangement for parallel/serial conversion (See Abstract and Figure), wherein

- at least one shift register (i.e., first shift register 1 and second shift register 2 in Figure) on an input port for storing data in memory (See col. 3, lines 43-46) and shifting data with larger bit length to a smaller bit length data (See col. 3, lines 62+; i.e., shifting D_{Pin} with larger parallel bit length to a smaller serial bit length D_{Sout} for Parallel/Serial conversion) for transmission from an input port with more width (i.e., a plurality of bits in parallel D_{Pin} in Figure) to an output port with less width (i.e., a serialized bits D_{Sout} in Figure).

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Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said parallel/serial conversion, as disclosed by Tauchen, in said each input port of said crossbar, as disclosed by Yokoyama, for the advantage of performing the conversion of said input data (e.g., 256 bit width data; i.e., parallel data) into (e.g., 1 bit width data in serial; i.e., serial data) without needing any external software or microprocessor control (See Tauchen, col. 4, line 66 through col. 5, line 8) in addition to the fixed bit width crossbar switching (i.e., crossbar switching between 256 bit width and 128 bit width; See Yokoyama, Figs. 1 and 24).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Aimoto [US 6,570,876 B1].

Referring to claim 5. Yokoyama discloses all the limitations of the claim 5, except that does not expressly teach at least one multiplexor device on each said input port and each said output port for prioritizing transmissions of data.

Aimoto discloses a packet switch and switching method (See col. 1, lines 8-16 and Fig. 1), wherein

- at least one multiplexor device (i.e., relaying priority control unit 3 and received packet queuing unit 7 of input port interface 20 in Fig. 1, and transmission priority control unit 5 and transmission packet queuing unit 8 of output port interface 21 in Fig. 1) on each input port (i.e., input port interface 20 of Fig. 1) and each output port (i.e., output port interface 21 of Fig. 1) for prioritizing transmissions of data (See col. 5, line 42 through col. 6, line 46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said multiplexor device, as disclosed by Aimoto, in said each input port of said crossbar, as disclosed by Yokoyama, for the advantage of providing crossbar switching (i.e., packet switching) that can perform both bandwidth control and priority control according to the communication protocol of variable length data (i.e., packet; See Aimoto, col. 2, lines 23-26).

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Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] as applied to claims 1, 3, 6-8 and 11-13 above, and further in view of Hsieh et al. [US 5,717,871 A; cited by the Applicant; hereinafter Hsieh].

Referring to claim 10. Yokoyama discloses all the limitations of the claim 10, except that does not expressly teach said crossbar control data contain control information for use by any one from the group of a shift register or a multiplexor device.

Hsieh discloses a programmable port for crossbar switch 10 in Fig. 1, wherein

- said programmable port receiving crossbar control data (See col. 9, lines 34-36) contain control information (See col. 9, lines 39-41) for use by any one from the group of a shift register (i.e., shift register 20 of Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said programmable port, as disclosed by Hsieh, on said each port of said crossbar, as disclosed by Yokoyama, for the advantage of providing a port flexibility in the use of control inputs and reduces the number of crossbar switch control inputs required to implement various modes of port operation (See Hsieh, col. 2, lines 43-49).

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama [JP 411296473 A] in view of what was well known in the art, as exemplified by Lach [US 6,363,452 B1].

Referring to claim 16. Yokoyama discloses a system (i.e., crossbar switching system including in Fig. 1) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), wherein said crossbar includes a plurality of ports (i.e., ports for Processor Boards #1-#2,

Memory Boards #1-#2, and DA I/O Board #1-#4 in Fig. 1), each port capable of being an input port customized (See Figs. 3 and 11; i.e., SW#2 being set '1' and SW#3 being set '1' make the port customize as an input port in Fig. 3) for receiving data from a source agent (i.e., receiving data from Processor Board in Fig. 1) and an output port customized (See Figs. 3 and 11; i.e., SW#2 being set '0' and SW#3 being set '0' make the port customize as an output port in Fig. 3) for transferring data to a destination agent (i.e., transferring data to DA I/O port in Fig. 1), and crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for indicating crossbar control information (i.e., Crossbar Switching control information) for transmitting data from an input port to an output port (See Figs. 25-38) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example), comprising:

- a storage medium (i.e., memory A 61b-1, and memory B 61c-1 in Fig. 9);
- a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and
- a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1),
- said machine comprising a set of flow steps for:
 - receiving data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3);
 - obtaining a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and

7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively);

- determining whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration);
- obtaining control information from said crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13);
- processing said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]);
- determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board);
- submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data);
- obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining

whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example);

- o formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]);
- o submitting said formatted data as said processed data; and, transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps.

The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps, as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

Referring to claim 17, Yokoyama discloses a machine (i.e., means for switching in crossbar switch 5 of Fig. 1 for executing the flows in Figs. 12-15 and 17-23) for transmitting data between customized ports (e.g., ports for DA I/O Board #1-#4 in Fig. 1 configured as output ports, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) and a plurality of system agents (e.g., Processor Boards #1-#2, and Memory Boards #1-#2 in Fig. 1) in a processing system via a crossbar (i.e., Crossbar Switch 5 of Fig. 1), said machine comprising a set of flow steps to:

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- receive data (See Box S1 in Fig. 12 and col. 15, lines 39-45) on an input port (e.g., port for Processor Board #1 of which both of SW#2 and SW#3 are set '1', i.e., making the port customize as an input port in Fig. 3);
- obtain a destination output port (i.e., port configured as an output port, which is designated by Address in Fig. 1) for said data received on said input port (i.e., said received transfer request data including Data processed by Data division 7-1, 7-2, 7-3 and 7-4, and Address processed by Address Controller 8-1, 8-2, 8-3 and 8-4 in Fig. 1, respectively);
- determine whether said input port has the same configuration as said output port (See Decision Box S2 and Decision Box S6 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration);
- obtain control information from a crossbar control data when said input port does not have the same configurations as said output port (See Box S5 and Decision Box S6 in Fig. 12 and col. 16, lines 11-13);
- process said data according to said obtained control information from said crossbar control data (See Box S12 in Fig. 12, Decision Box S18, Box S19 and S20 in Fig. 14 and paragraph [0094]);
- determining whether a width of said input port (See Decision Block S2 in Fig. 12; i.e., is the input port 256 bit configuration board ?) is more than a width of said output port (See Decision Block S6 in Fig. 12; e.g., if the communication partner is 128 bit configuration board);
- submitting said data as a processed data when said width of said input port is not more than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and submitting 256 bit configured data as a processed data);

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- obtaining said width of said output port when said width of said input port is greater than said width of said output port (See Decision Box S2, Decision Box S6 and Box S9 in Fig. 12 and col. 15, lines 45-47 and col. 16, lines 7-11 and 14-20; i.e., determining whether said input port has 256 bit configuration as said output port having 256 bit configuration, and obtaining 128 bit configured data width, for example);
- formatting said data from said input port to data configured for said obtained width of said output port (See Box S20 in Fig. 14 and paragraphs [0090]-[0091]); and
- submitting said formatted data as said processed data; and, transmitting said processed data to a destination output port (See Box S21 in Fig. 14 and col. 17, lines 10-14).

Yokoyama does not expressly teach said machine comprising a set of instructions for said flow steps.

The Examiner takes Official Notice that said flow steps could be achieved in all software implementation (i.e., instructions) with the same or equivalent results, using appropriate program codes (i.e., processor instructions), is well known to one of ordinary skill in the art, as evidenced by Lach, at col. 12, lines 3-9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said flow steps, as disclosed by Yokoyama, in software since it would allow a better flexibility of an implementation than a hardware implementation.

(10) Response to Argument

In response to the Appellant's argument with respect to the argument "The §112, Second Paragraph Rejection of Claims 12, 16 and 17 Should be Reversed Because of Applicant's use of the Recitation 'the Width of the Input Port' and 'the Width of the Output Port' is not indefinite." in the Appeal Brief on page 3, the Examiner withdraws the claims 12, 16, 17 rejection under 35 U.S.C. §112, second paragraph according to the persuasive argument.

Refer to WITHDRAWN REJECTIONS in the item (6) Grounds of Rejection to be Reviewed on Appeal.

In response to the Appellant's argument with respect to "With regard to the examiner's rejections, it is noted that the undersigned had a telephone interview with the examiner on September 1, 2004, in which the principal reference of Yokoyama was discussed. ... The examiner indicated that he did read Japanese and also informed applicant that the Japanese Patent Office had a free computer translation system in which an English translation could be obtained and offered to acquire and fax the English translation to applicant, which was done. ... The undersigned wishes to point out that the translation was indeed difficult to understand and that the examiner has also relied on descriptions of text contained in drawings which applicant is unable to verify the accuracy of or at least fully consider. Applicant formally requested that if the amendments that are made herein were unsuccessful and if Yokoyama continued to be a basis for rejection of the claims of this application, an accurate translation from the USPTO should be provided to applicant. The USPTO did not supply any additional translation. Because applicant believed that he was disadvantaged by the potential of an incorrect translation, a separate translation was ordered. The second translation was of little assistance. ..." in the Appeal Brief on page 4, line 9 through page 5, line 7, the Examiner notices that this issue should be related to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

Essentially, the Appellant is concerned about any potential disadvantages caused by the potential of an incorrect translation. However, the Examiner stresses that (1) Yokoyama was filed on 7th of July 2003 as an IDS (PTO-1449) by the Appellant, (2) the Office provided the English translation copy of Yokoyama on 1st of September 2004 for the convenience of the Appellant via FAX, (3) the Office does not have any obligatory promise to provide a certified translation service to the Applicant as long as the Office provides a translation copy of reference being used for final claim rejections, (4) the Appellant admitted that the separate translation being ordered by the Appellant was of little assistance, and (5) the most important thing is that this issue is not to appealable subject matter, but to petitionable subject matter under 37 CFR 1.181.

In other words, the Examiner has been presumed that the Appellant fully understands the claim rejections by Yokoyama because (1) Yokoyama was filed by the Appellant as a relevant prior art via the IDS, and (2) Appellant obtained two different versions of Yokoyama translation in English.

Even though the Appellant asserts that Yokoyama was provided by the EPO which consisted of less than a full page of description relating to the nature of the operation of the Yokoyama system, the Examiner believes the Appellant should further pay attention to the full-copy of Yokoyama for obviating any potential disadvantages caused by misinterpretation/misunderstanding of Yokoyama because Yokoyama was used for the claim rejections.

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to "With regard to amended claim 1, the examiner's position with regard to Yokoyama anticipating the following element recitation: ... was that setting switches 2 and 3 make the port configure as an output port according to Figs. 3 and 11, with less width than said input port and cites Fig. 24 and paragraph 0149. The examiner's reliance on Fig. 24 is not

instructive as it merely shows a table of control numbers, i.e., C1 through C9, which essentially seems to show that a 256 bit band can be secured for transmitting 128 bit or 256 bit data, with paragraph 0149 reading "C6 shows the case where 128 bit band can be secured in case 256 bit data are transmitted to a 128 bit port and in case C7 transmits 256 bit data to 128 bit port, it shows the case where a band is not securable." Nowhere else in the specification, to the extent that applicant can understand it, is there any discussion that data is formatted at all. ... There is no discussion why or how case C6 differs from case C7 anywhere in the 25 page translation. It is submitted that the described case C6 is either gratuitous or erroneous. Nowhere in the specification does it indicate that data is reformatted to fit the width of the output port if the output port capacity is less than that of the input port." in the Appeal Brief on page 5, line 8 through page 6, line 3, the Examiner respectfully disagrees.

In fact, Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1), wherein it anticipates

- crossbar control data (i.e., discernment bits Sa and Sb, and Address in Fig. 2) for specifying crossbar control information (i.e., Crossbar Switching control information) for transferring data from an input port to an output port (i.e., from input port coupled to 256 bit board to output port coupled to 128 bit board in Fig. 1) having different port configurations (i.e., having 128 bit and 256 bit port configurations; See Paragraphs [0148], [0149], [0154], and [0155], as an example),
 - said crossbar control data (i.e., said discernment bits Sa and Sb, and Address) containing control information for **formatting** bit length of data (i.e., control information for configuring bit length 128 bit or bit length 256 bit port; See Fig. 24, wherein in fact, 256 bit port → 128 bit port inherently anticipates **formatting** bit length of data. In other words, the 256 bit length of data from the input port is **formatted** to the 128 bit length of data to output port) from an input port (e.g., port for Processor Boards #1-#2 and Memory Boards #1-#2 in Fig. 1 configured as an input port, such that SW#2 being set '1' and

SW#3 being set '1' make the port configure as an input port according to Figs. 3 and 11) to be transmitted to an output port (e.g., port for DA I/O Board #1-#4 in Fig. 1 configured as an output port, such that SW#2 being set '0' and SW#3 being set '0' make the port configure as an output port according to Figs. 3 and 11) having less width than said input port (i.e., 256 bit port → 128 bit port in Fig. 24; See Paragraph [0149]).

Therefore, in contrary to the Appellant's argument, Yokoyama fully discloses that data is **formatted**, i.e., changing the bit length format, in the specification. It is particularly mentioned at paragraph [0019] of Yokoyama.

Furthermore, the Appellant asserts that there is no discussion why or how case C6 differs from case C7 anywhere in the 25 page translation. In contrary to the Appellant's assertion, Yokoyama clearly discusses that case C6 shows the case where a band of 128 bits can be secured when data of 256 bits are transferred to a 128-bit port, and C7 shows the case where a band cannot be secured when data of 256 bits are transferred to a 128-bit port in the paragraph [0149]. In other words, the cases C6 and C7 show when data of 256 bits are transferred to a 128-bit port, respectively. However, in case of C6, the data of 256 bits are successfully transferred to a 128-bit port after changing the bit length format, i.e., **being formatted**, and, in case of C7, the data of 256 bits cannot be transferred to a 128-bit port because of said unsecured band. Therefore, the Appellant's assertion, i.e., the described case C6 is either gratuitous or erroneous, is incorrect.

Thus, Appellant's argument for these points cannot be seen as persuasive.

In response to the Appellant's argument with respect to "Claim 11 is also believed to be allowable for the reason that Yokoyama totally fails to anticipate, teach or suggest a crossbar having a plurality of virtual communication channels on each input port. The examiner attempts to equate a plurality of virtual communication channels on each input port to data paths that are provided by the interconnection of

switches in Fig. 5. Applicant believes that this is a totally misplaced reliance on the switch configuration shown in Fig. 5. It has nothing to do with virtual communication channels that are claimed.” in the Appeal Brief page 6, lines 4-10, the Examiner respectfully disagrees.

In fact, Yokoyama discloses a crossbar (i.e., crossbar switching system in Fig. 1), wherein it anticipates

- a plurality of virtual communication channels (i.e., a plurality of data paths by the interconnection of switches in Fig. 5) on each input port (i.e., on each data division 7-1 of Fig. 3).

Therefore, in contrary to the Appellant's argument, Yokoyama clearly anticipates that a plurality of virtual communication channels on each input port (i.e., a plurality of data paths by the interconnection of switches on each data division of processor boards). In other words, a plurality of data paths are virtually interconnected by switches on each data division of processor boards.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to “Claim 12 is also believed to be allowable over Yokoyama essentially for the same reasons as set forth above with regard to claim 1.” in the Appeal Brief page 6, lines 11-12, the Examiner respectfully disagrees.

As is discussed above, Yokoyama anticipates all the limitations of the claim 1. Furthermore, the claim 12 is also anticipated by Yokoyama, which is shown in the item (9) Grounds of Rejection. Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to “The examiner's position with regard to the amendatory language that was added to claims 16 and 17 (and to claim 12), namely: ... was that Yokoyama meets the formatting step by Box S20 in Fig. 14, which is untranslated Japanese text that appears to be unimportant, and paragraphs 0090-0091. Paragraphs 0090-0091 in the computer-generated

translation read as follows: ... Clearly, these paragraphs cited by the examiner have nothing to do with the step of processing the data which comprises the steps of determining ..., submitting ..., obtaining ...; and formatting This is simply not done by Yokoyama. As can be best understood, Yokoyama transmits 128 bit data or 256 bit data through ports that ... There is no discussion that has been located which indicates that data is **reformatted** so that it is configured for the obtained width of the output port." in the Appeal Brief on page 6, lines 15 through page 8, line 3, the Examiner respectfully disagrees.

First of all, in contrary to the Appellant's statement, Yokoyama suggests formatting data from input port to data configured for obtained width of output port at the Step Box S20 in Fig. 14, wherein the Step Box S20 states "when the address controller part in the board replies OK, record the secured path and the correspondence information in the memory B." This is further detailed in the paragraphs [0090]-[0091]. The flowchart (B) in Fig. 14 is performed when the input port 256 bits (See the Step Box S2 in Fig. 12) and the output port 128 bits (See the Step Box S6 in Fig. 12; in fact, other than 256 bit corresponding board), i.e., proceeding to flowchart (B) in Fig. 14. In the flowchart (B) in Fig. 14, the Step Box S20 is performing the configuration of bit-length changing from 256 bits to 128 bits, i.e., formatting, by way of recording the secured path and the correspondence information in the memory B.

Furthermore, it is noted that the features upon which appellant relies (i.e., reformatting) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to "The examiner cites col. 12, lines 3-9 of Lach for the proposition that he takes Official Notice that flow steps can be implemented with the "same or equivalent results" and is well known to those of ordinary skill in the art. ... The examiner ignores the

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fact that Yokoyama fails to teach or suggest the flow steps themselves and Lach simply fails to supply the basic deficiency of Yokoyama. The examiner's Official Notice does not help him." in the Appeal Brief page 6, lines 11-12, the Examiner respectfully disagrees.

As is discussed above, Yokoyama anticipates all the limitations of the claim 1. Furthermore, the claim 16 is also suggested by Yokoyama, except that Yokoyama does not expressly teach the machine comprising a set of instructions for the claimed flow steps. However, the Examiner notices that it was well known in the art, and the evidence was exemplified by Lach in the Office Actions, which is shown in the item (9) Grounds of Rejection.

Thus, Appellant's argument for this point cannot be seen as persuasive.

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(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

CEL/ 

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